CLAIMS

We claim:

1. A method for programming non-volatile memory, comprising:

performing one or more programming operations on a non-volatile storage element;

determining that said non-volatile storage element has reached an intermediate verify threshold, said intermediate verify threshold is different than a final verify threshold;

performing only one additional programming operation at a reduced level on said non-volatile storage element in response to said step of determining; and

inhibiting programming of said non-volatile storage element after performing said only one additional programming operation regardless of change in threshold voltage for said non-volatile storage element in response to said one additional programming operation.

2. A method according to claim 1, wherein:

said one or more programming operations include applying programming pulses which increase in magnitude at a step size; and

said one additional programming operation intentionally changes a threshold voltage of said non-volatile storage element by an amount approximately half of said step size.

3. A method according to claim 1, wherein:

said intermediate verify threshold is below said final verify threshold by an amount such that after said non-volatile storage element has reached said intermediate

verify threshold said one additional programming operation will cause said non-volatile storage element to reach or almost reach said final verify threshold.

4. A method according to claim 1, wherein:

said one or more programming operations are performed while a bit line voltage for said non-volatile storage element is at a programming level;

said inhibiting programming of said non-volatile storage element is performed while said bit line voltage for said non-volatile storage element is at an inhibit level; and

said one additional programming operation is performed while said bit line voltage for said non-volatile storage element is at an intermediate level between said programming level and said inhibit level, said bit line voltage for said non-volatile storage element is at said intermediate level for exactly one programming operation.

5. A method according to claim 1, wherein:

said one additional programming operation is performed at said reduced level by raising a bit line voltage for said non-volatile storage element.

6. A method according to claim 1, wherein:

said one or more programming operations include applying programming pulses; and

said one additional programming operation is performed at said reduced level by reducing the width of a programming pulse for said one additional programming operation.

7. A method according to claim 1, wherein:

said one or more programming operations include applying programming pulses;

said step of performing only one additional programming operation includes

applying one programming pulse; and

said step of inhibiting is required to be performed after applying said one programming pulse.

8. A method for programming non-volatile memory, comprising:

performing one or more programming operations on non-volatile storage elements;

determining which of said non-volatile storage element reached an intermediate verify threshold but have not reached a final verify threshold;

performing one additional programming operation at a reduced level on said non-volatile storage elements that have reached said intermediate verify threshold but have not reached said final verify threshold;

for said non-volatile storage elements that have reached said intermediate verify threshold but have not reached a final verify threshold, automatically inhibiting programming after said one additional programming operation; and

continuing programming for non-volatile storage elements that have not reached said intermediate verify threshold.

9. A method according to claim 8, wherein:

said one or more programming operations include applying programming pulses which increase in magnitude at a step size; and

for said non-volatile storage elements that have reached said intermediate verify threshold but have not reached said final verify threshold, said one additional programming operation intentionally changes threshold voltages by an amount approximately half of said step size.

10. A method according to claim 8, wherein:

said intermediate verify threshold is below said final verify threshold by an amount such that for non-volatile storage elements that have reached said intermediate verify threshold said one additional programming operation will cause said non-volatile storage element to reach or almost reach said final verify threshold.

11. A method according to claim 8, wherein:

said one or more programming operations are performed while bit line voltages for said non-volatile storage elements are at a programming level range;

said inhibiting programming is performed while bit line voltages are at an inhibit level; and

said one additional programming operation is performed while bit line voltages are at an intermediate level between said programming level and said inhibit level.

12. A method according to claim 11, wherein:

said one or more programming operations include applying programming pulses;

said step of performing only one additional programming operation includes applying one programming pulse; and

said step of inhibiting is required to be performed after applying said one programming pulse.

13. A method according to claim 8, wherein:

said one or more programming operations include applying programming pulses;

said step of performing only one additional programming operation includes applying one programming pulse; and

said step of inhibiting is required to be performed after applying said one programming pulse.

14. A method according to claim 8, wherein:

said one or more programming operations include applying programming pulses; and

said one additional programming operation is performed at said reduced level by reducing a width of a programming pulse for said one additional programming operation.

15. A non-volatile storage system, comprising:

an array of non-volatile storage elements; and

a control circuit in communication with said non-volatile storage elements, said control circuit causes said non-volatile storage elements to perform one or more programming operations, determines which of said non-volatile storage element reached an intermediate verify threshold but have not reached a final verify threshold, causes one additional programming operation at a reduced level to be performed on said non-volatile storage elements that have reached said intermediate verify threshold but have not reached said final verify threshold, inhibits programming for said non-volatile storage elements that have reached said intermediate verify threshold after said one additional programming operation and continues programming for non-volatile storage elements that have not reached said intermediate verify threshold, said control circuit is required to inhibit programming for said non-volatile storage elements that have reached said intermediate verify threshold after said one additional programming operation and prior to additional programming operations.

16. A non-volatile storage system according to claim 15, wherein:

said control circuit includes a controller.

17. A non-volatile storage system according to claim 15, wherein:

said control circuit includes a state machine.

18. A non-volatile storage system according to claim 15, wherein:

said control circuit includes a set of sense amplification circuits, a controller and a state machine.

19. A non-volatile storage system according to claim 15, wherein:

said one or more programming operations include programming pulses which increase in magnitude at a step size; and

for said non-volatile storage elements that have reached said intermediate verify threshold but have not reached said final verify threshold, said one additional programming operation intentionally changes threshold voltages by an amount approximately half of said step size.

20. A non-volatile storage system according to claim 15, wherein:

said one or more programming operations are performed while bit line voltages for said non-volatile storage elements are at a programming level range;

said inhibiting programming is performed while bit line voltages are at an inhibit level range; and

said one additional programming operation is performed while bit line voltages are at an intermediate level range between said programming level range and said inhibit level range.

21. A non-volatile storage system according to claim 15, wherein:

said one or more programming operations include applying programming pulses; and

said one additional programming operation includes applying one programming pulse.

22. A method for programming non-volatile memory, comprising:

performing programming operations on a non-volatile storage element, said programming operations include an increasing program voltage, said increasing program voltage has an increment size;

determining that said non-volatile storage element has reached a particular intermediate verify threshold of a set of one or more intermediate verify thresholds;

performing one additional programming operation on said non-volatile storage element in response to said step of determining, said one additional programming operation changes a threshold voltage of said non-volatile storage element by a fraction of said increment size, wherein size of said fraction depends on which of said intermediate verify thresholds had been determined to be reached; and

inhibiting programming of said non-volatile storage element after performing said one additional programming operation, said step of inhibiting is required to be performed after said one additional programming operation and prior to other additional programming operations.

23. A method according to claim 22, wherein:

said fraction of said increment size is half of said increment size and

said set of one or more intermediate verify thresholds includes one intermediate verify threshold.

24. A method according to claim 22, wherein:

said fraction of said increment size is one third of said increment size; and

said set of intermediate verify thresholds includes two intermediate verify thresholds.

25. A method according to claim 22, wherein:

said fraction of said increment size is two thirds of said increment size; and

said set of intermediate verify thresholds includes two intermediate verify thresholds.

26. A method according to claim 22, wherein:

said set of intermediate verify thresholds includes three or more intermediate verify thresholds.

27. A method according to claim 22, wherein:

said programming operations are performed while a bit line voltage for said non-volatile storage element is at a programming level;

said inhibiting programming is performed while said bit line voltage is at an inhibit level; and

said one additional programming operation is performed while said bit line voltage is at an intermediate level between said programming level and said inhibit level.

28. A method according to claim 22, wherein:

said one or more programming operations include applying programming pulses;

said one additional programming operation includes applying one programming pulse; and

said inhibiting is required to be performed after applying said one programming pulse.

29. A non-volatile storage system, comprising:

an array of non-volatile storage elements;

a control circuit in communication with said non-volatile storage elements, said

control circuit causes said non-volatile storage elements to perform one or more programming operations, determines which of said non-volatile storage element reached an intermediate verify threshold but have not reached a final verify threshold, causes one additional programming operation at a reduced level to be performed on said non-volatile storage elements that have reached said intermediate verify threshold but have not reached said final verify threshold, inhibits programming for said non-volatile storage elements that have reached said intermediate verify threshold automatically after said one additional programming operation; and

wherein said one or more programming operations include an increasing program voltage, said increasing program voltage has an increment size, said one additional programming operation changes threshold voltages by a fraction of said increment size based on said particular intermediate verify threshold.

30. A method according to claim 29, wherein:

said one or more programming operations are performed while bit line voltages for said non-volatile storage elements are at a programming level range;

said inhibiting programming is performed while said bit line voltages are at an inhibit level range; and

said one additional programming operation is performed while said bit line voltages are at an intermediate level range between said programming level range and said inhibit level range.

31. A method according to claim 29, wherein:

said one or more programming operations include applying programming pulses;

said one additional programming operation includes applying one programming pulse; and

said inhibiting is required to be performed after applying said one programming

pulse.

32. A method for programming non-volatile memory, comprising:

performing one or more programming operations on a non-volatile storage element;

determining that said non-volatile storage element has reached an intermediate verify threshold; and

performing exactly one additional programming operation on said non-volatile storage element in response to said step of determining, said intermediate verify threshold is situated with respect to a final verify threshold such that said one additional programming operation is intended to cause said non-volatile storage element to reach or almost reach said final verify threshold.

33. A method for creating a non-volatile memory system, comprising:

creating an array of non-volatile storage elements;

setting a final verify threshold for a programming process; and

setting an intermediate verify threshold for said programming process so that after a set of one or more non-volatile storage elements reach said intermediate verify threshold one programming operation will cause said set of one or more non-volatile storage elements to reach or almost reach said final verify threshold.

34. A method according to claim 33, wherein:

said programming process includes a set of programming operations;

each programming operation includes an application of a programming pulse so that said programming process includes a set of programming pulses increasing in magnitude by a step size; and

said final verify threshold differs from said intermediate verify threshold by a

fraction of said step size.

35. A method according to claim 33, wherein:

said programming process includes a set of programming operations;

each programming operation includes an application of a programming pulse so that said programming process includes a set of programming pulses increasing in magnitude by a step size; and

said final verify threshold differs from said intermediate verify threshold by half of said step size.